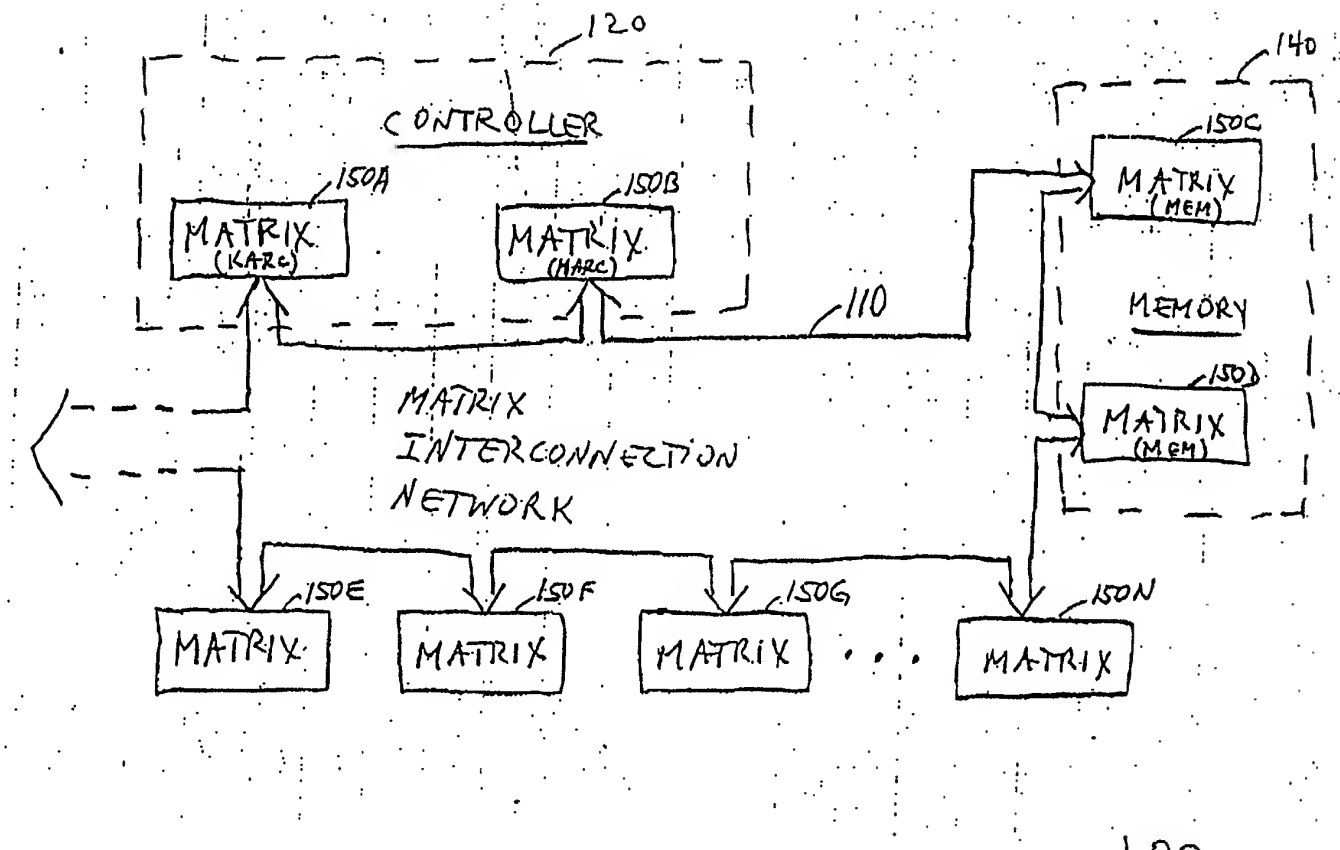
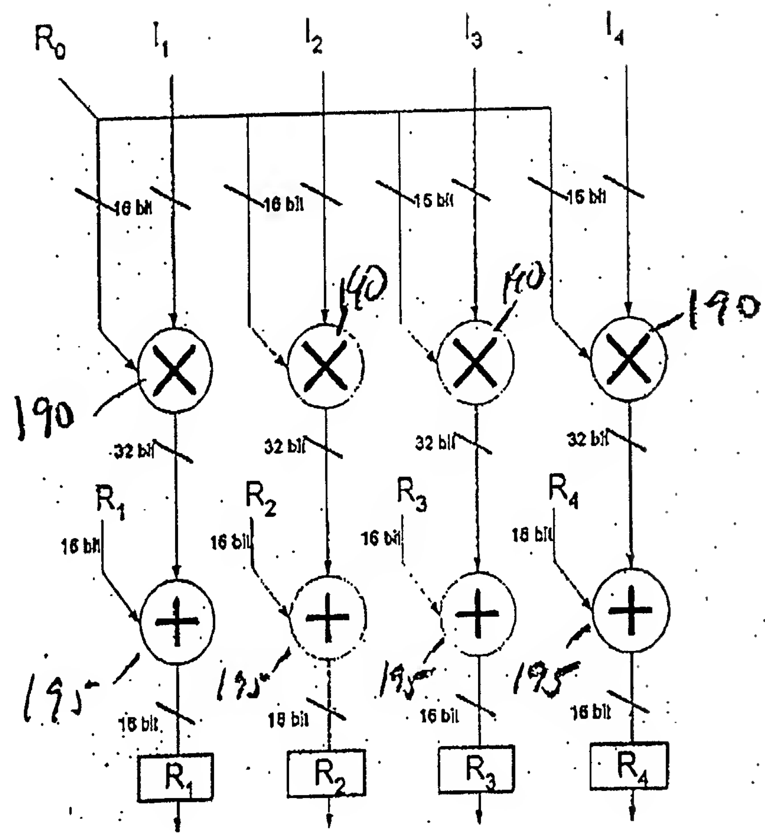


FIG. 1



R0
I1
I2
I3
I4
16 bit
16 bit
15 bit
15 bit
140
140
190
190
32 bit
32 bit
32 bit
32 bit
R1
R2
R3
R4
16 bit
16 bit
16 bit
16 bit
195
195
195
195
16 bit
16 bit
16 bit
16 bit
R1
R2
R3
R4

FIG. 2

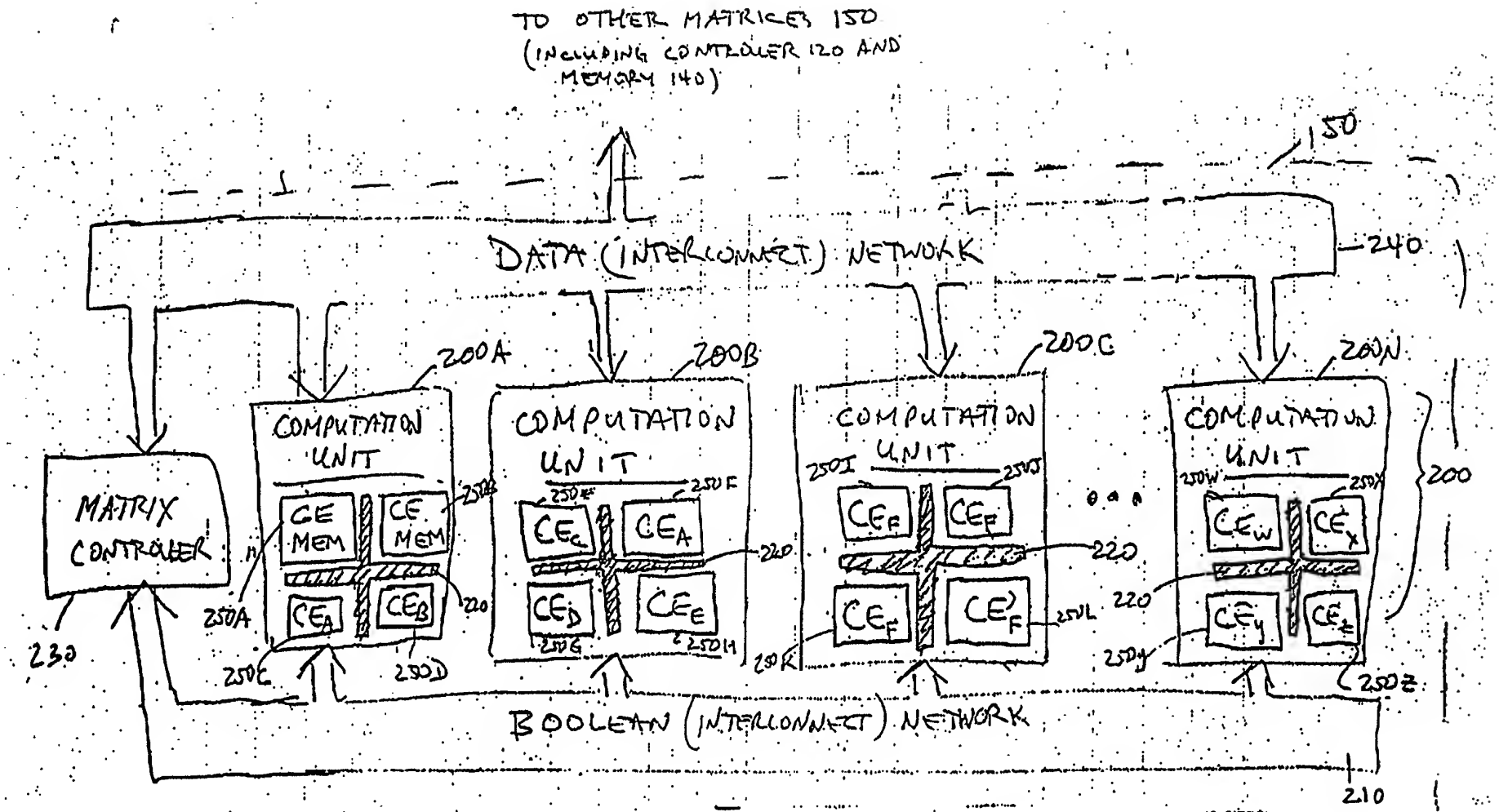


FIG. 3

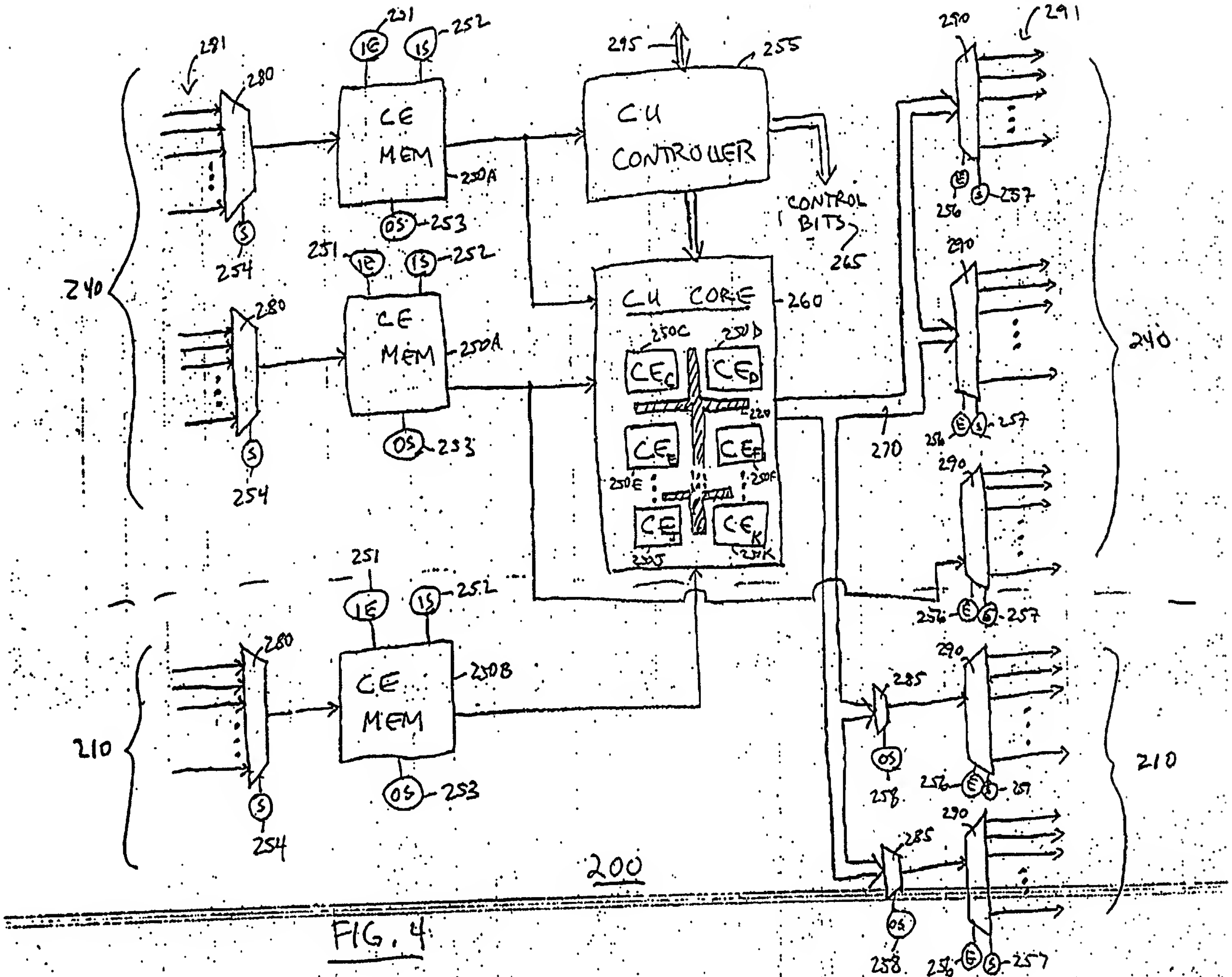

CE MEM
CE MEM
CE MEM
CU CONTROLLER
CU CORE
CONTROL BITS
CE C
CE D
CE E
CE F
CE J
CE K
1E
1S
OS
S
E
200
240
210
250A
250B
250C
250D
250E
250F
250J
250K
220
251
252
253
254
255
256
257
258
260
265
270
280
281
285
290
291
295

FIG. 4

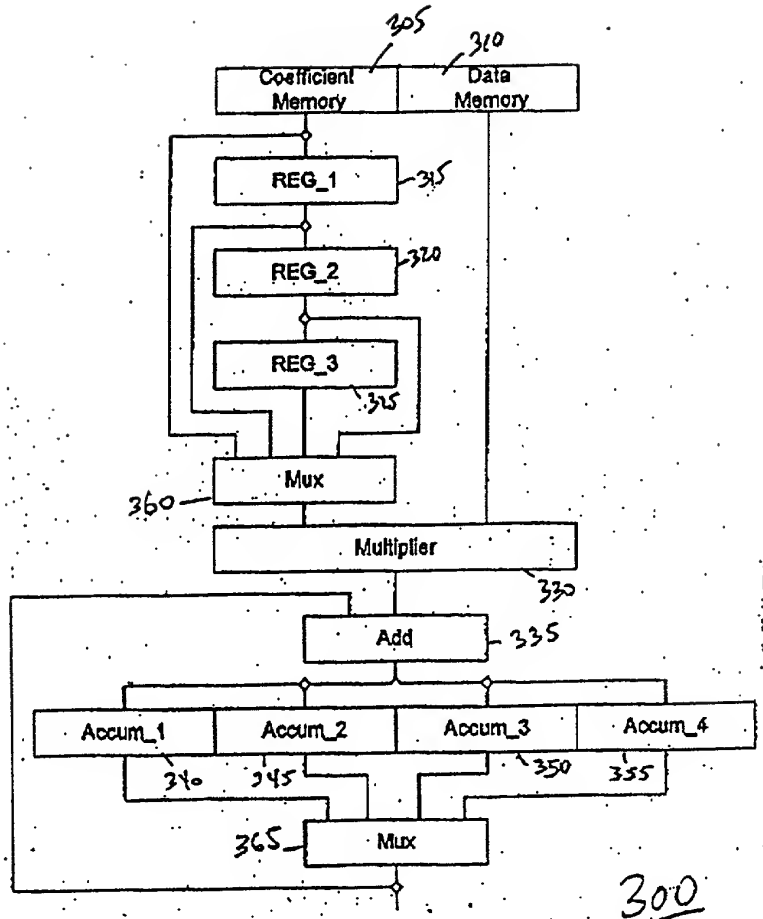

305
310
Coefficient Memory
Data Memory
REG_1
315
REG_2
320
REG_3
325
Mux
360
Multiplier
330
Add
335
Accum_1
Accum_2
Accum_3
Accum_4
340
345
350
355
365
Mux
300

FIG. 5A

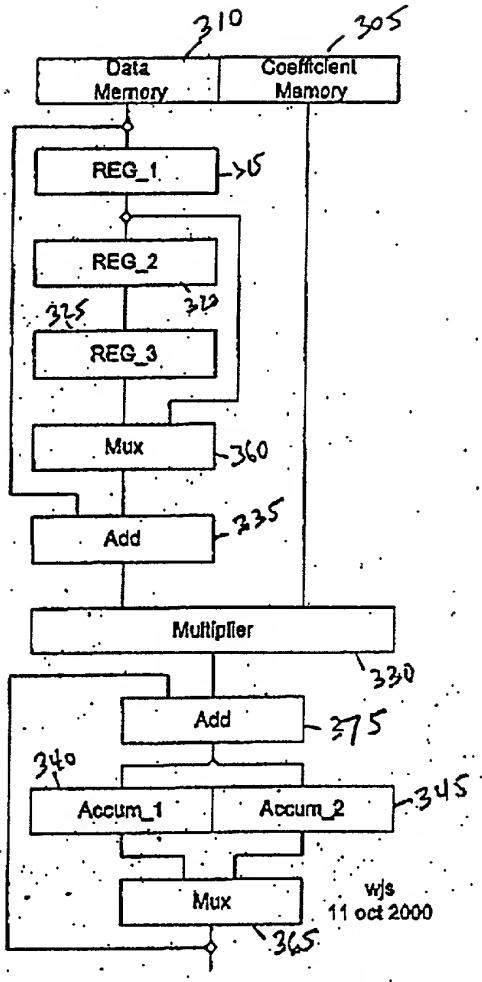
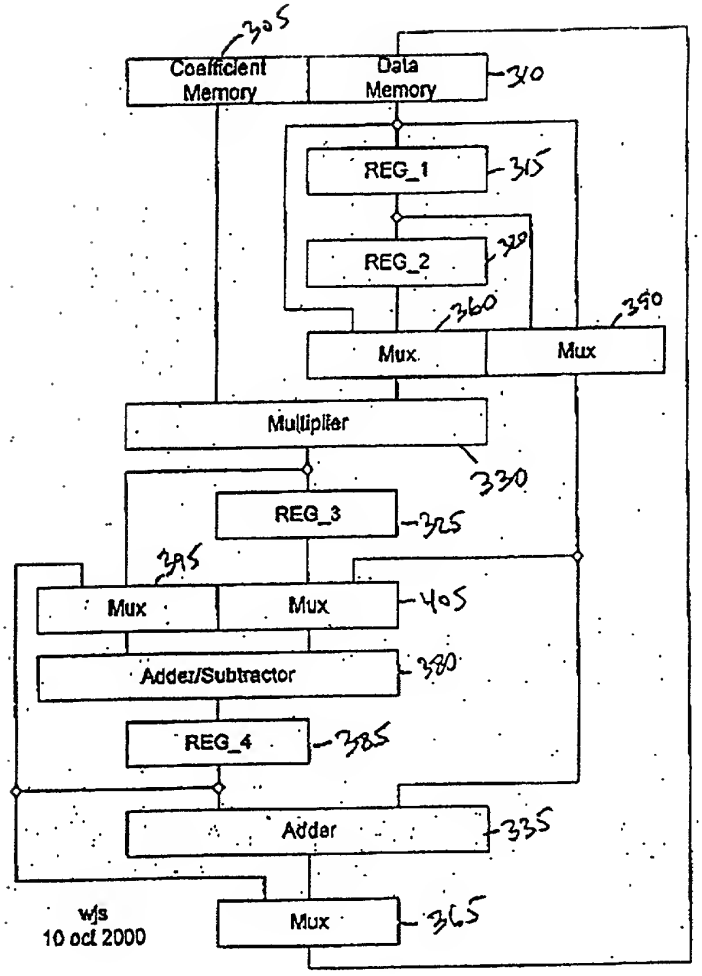
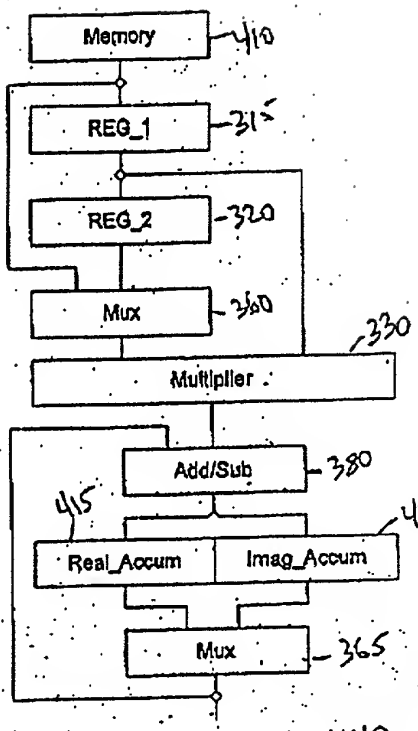

310
305
Data Memory
Coefficient Memory
REG_1
315
REG_2
325
320
REG_3
Mux
360
Add
335
Multiplier
330
Add
375
340
Accum_1
Accum_2
345
Mux
365
w/s
11 oct 2000
370

FIG. 5B


Coefficient Memory
Data Memory
REG_1
REG_2
Mux
Mux
Multiplier
REG_3
Mux
Mux
Adder/Subtractor
REG_4
Adder
Mux
w/s
10 oct 2000

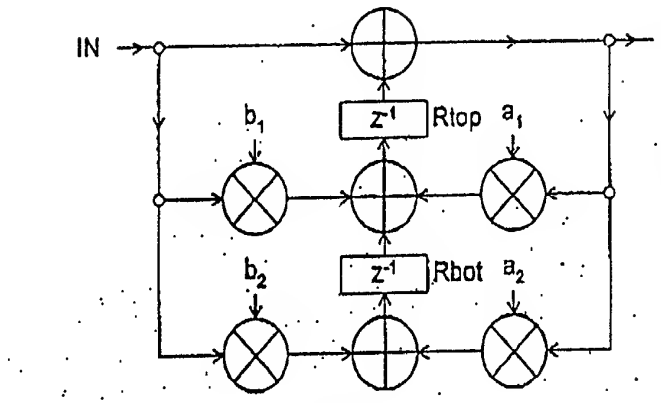
400

FIG. 5C



wjs
19 oct 2000

FIG. 5D



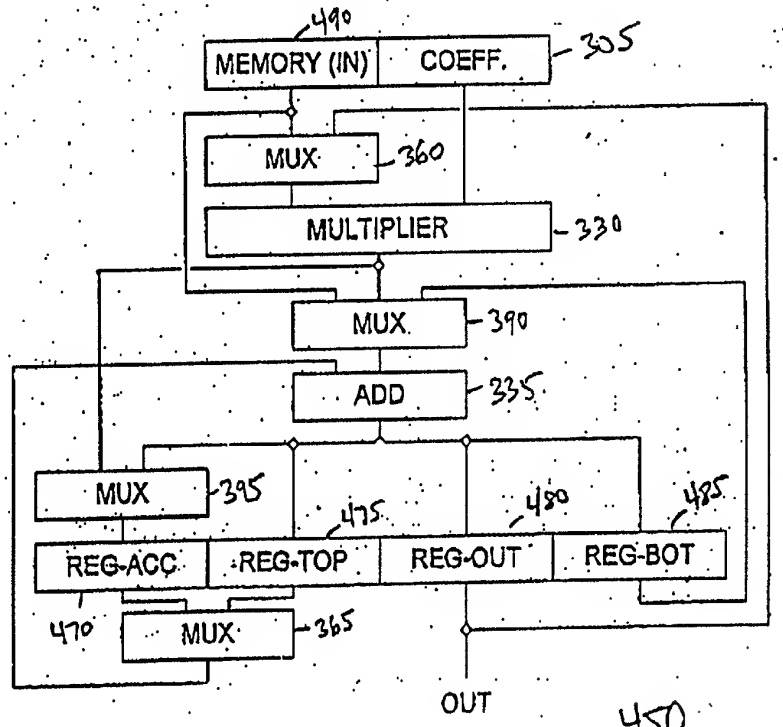
460

OUT <-- IN + Rtop

Rbot <-- IN * b_2 + OUT * a_2

Rtop <-- IN * b_1 + OUT * a_1 + Rbot

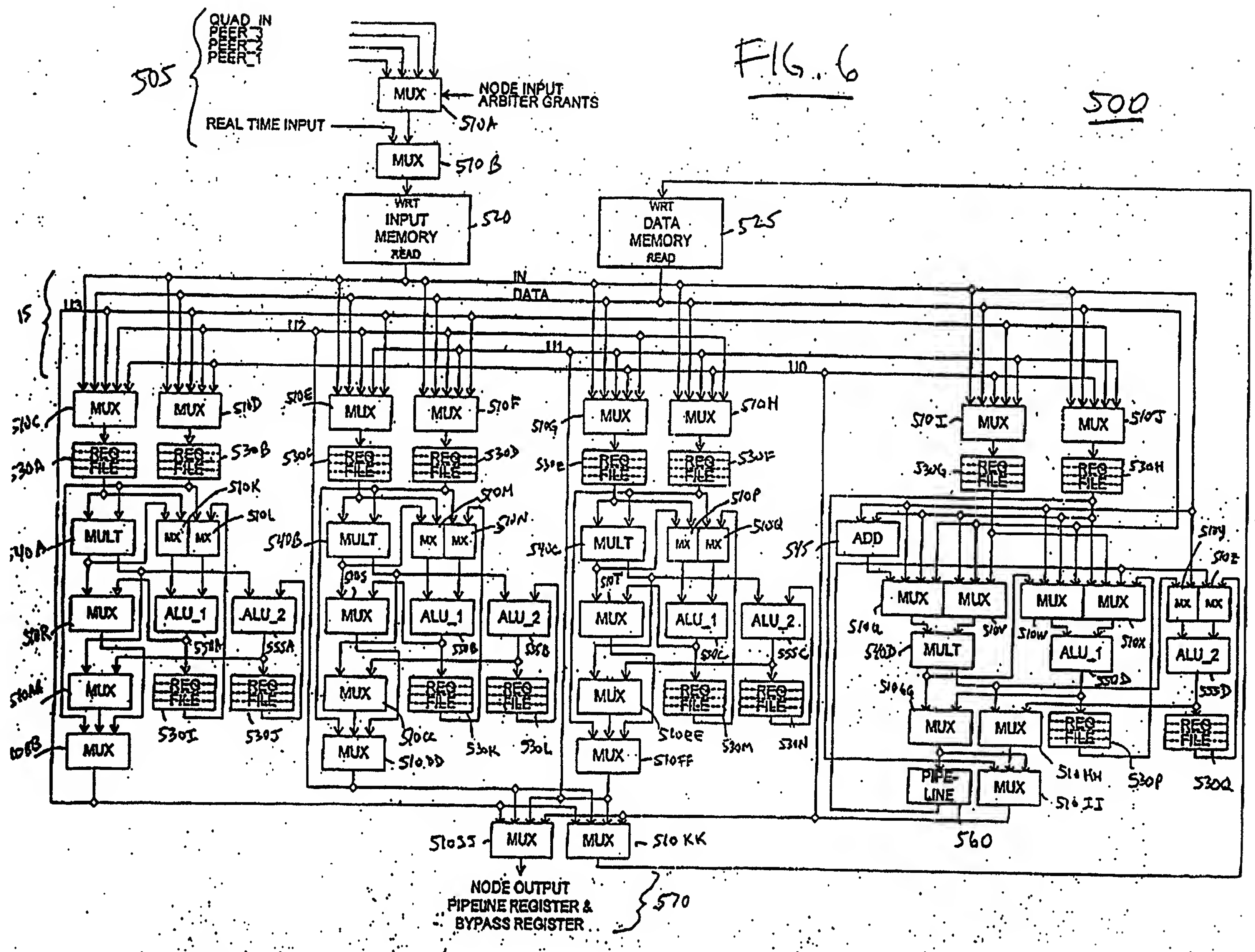
wjs
23 oct 2000



450

FIG. 5E

FIG. 6


500
505
QUAD_IN
PEER_3
PEER_2
PEER_1
REAL TIME INPUT
MUX
NODE INPUT ARBITER GRANTS
510A
510B
WRT
INPUT MEMORY
READ
520
DATA MEMORY
525
IN DATA
15
113
112
111
110
MULT
ALU_1
ALU_2
REG FILE
ADD
PIPE-LINE
560
515
510KK
510JJ
NODE OUTPUT PIPELINE REGISTER & BYPASS REGISTER
570

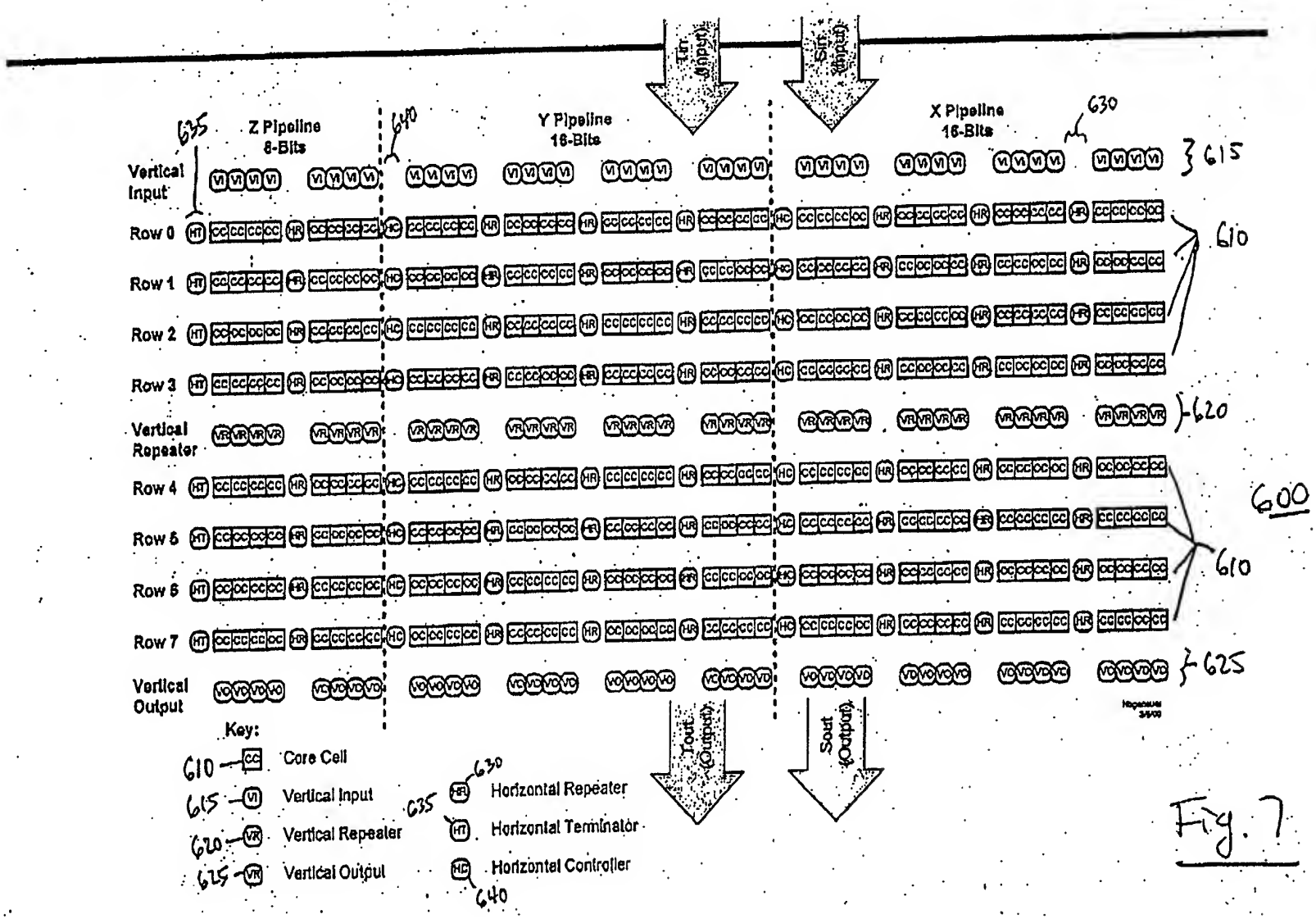

Tin (Input)
Sin (Input)
635
Z Pipeline 8-Bits
640
Y Pipeline 16-Bits
X Pipeline 16-Bits
630
Vertical Input
615
Row 0
Row 1
Row 2
Row 3
610
Vertical Repeater
620
Row 4
Row 5
Row 6
Row 7
610
600
Vertical Output
625
Tout (Output)
Sout (Output)
Key:
610 Core Cell
615 Vertical Input
620 Vertical Repeater
625 Vertical Output
630 Horizontal Repeater
635 Horizontal Terminator
640 Horizontal Controller

Fig. 7

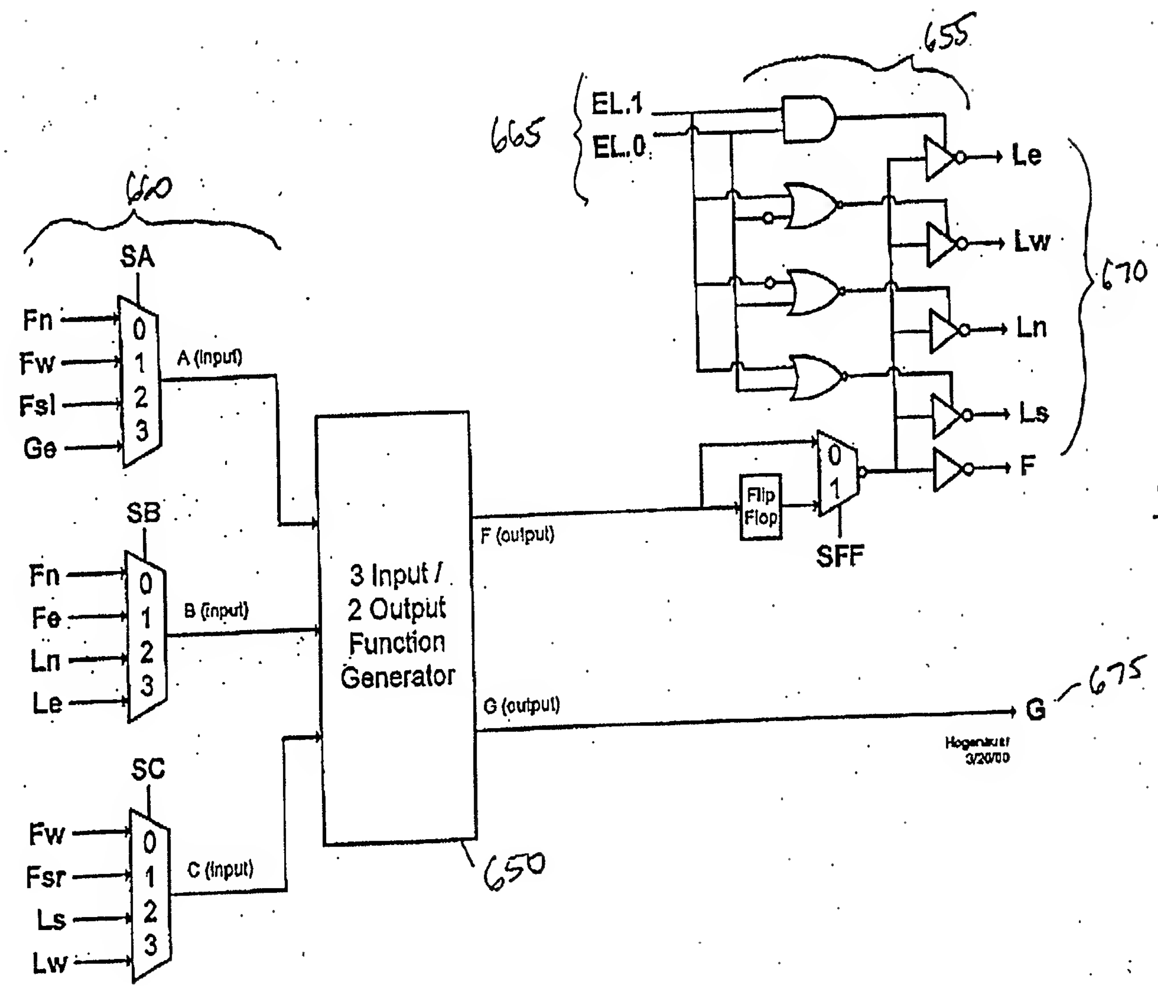

SA
Fn
Fw
Fsl
Ge
0
1
2
3
A (input)
SB
Fn
Fe
Ln
Le
B (input)
SC
Fw
Fsr
Ls
Lw
C (input)
3 Input / 2 Output Function Generator
F (output)
G (output)
EL.1
EL.0
Flip Flop
SFF
Le
Lw
Ln
Ls
F
G
660
665
655
670
650
675
610

Fig. 8

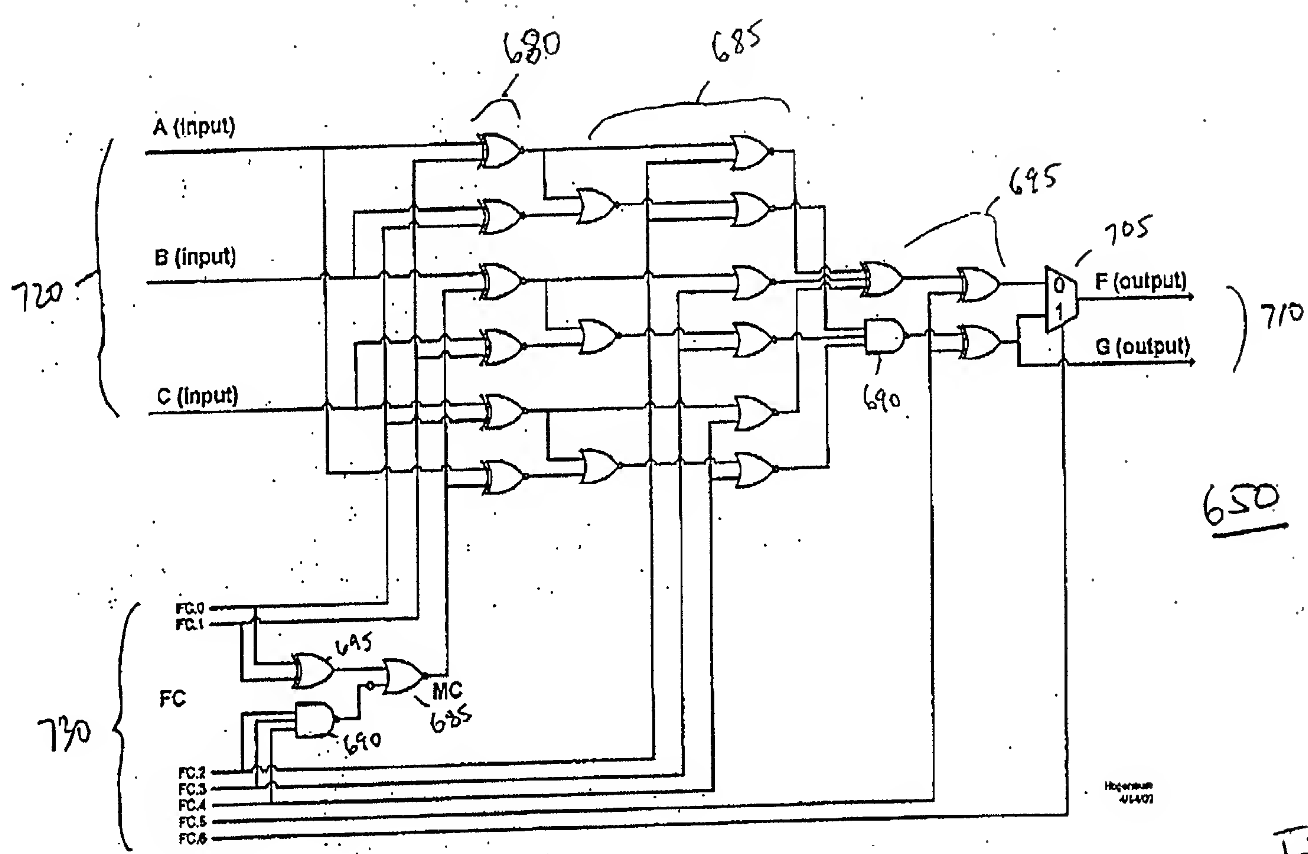

680
685
695
705
A (input)
B (input)
C (input)
720
F (output)
G (output)
710
690
650
FC.0
FC.1
FC
695
MC
685
690
730
FC.2
FC.3
FC.4
FC.5
FC.6

Fig. 9


1002
Searcher 1
1004
Searcher 2
1006
Searcher 3
At power-up
1002
Searcher 1
1008
Communicat function
After system acquisition

FIG. 10

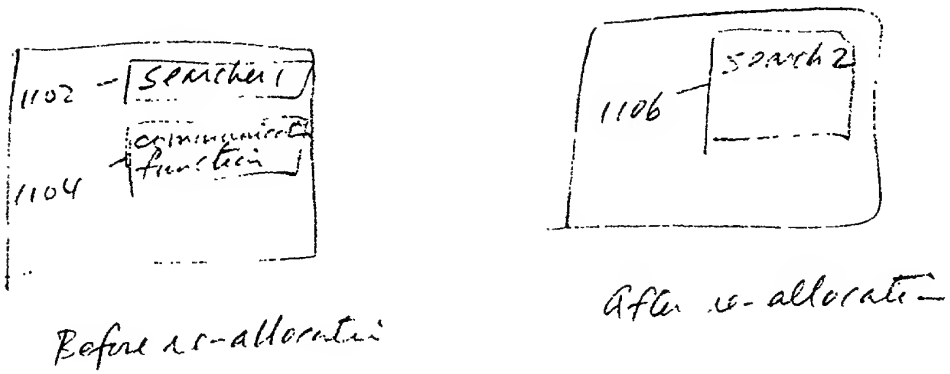

1102
Searcher 1
1104
1106
search 2
Before re-allocation
After re-allocation

FIG. 11

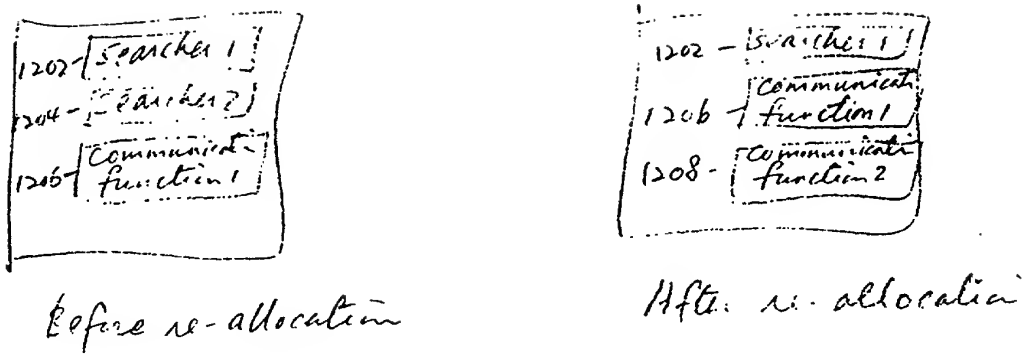

1202
Searcher 1
1204
Searcher 2
1206
Communicati-
function 1
Before re-allocation
1202
Searcher 1
1206
Communicati-
function 1
1208
Communicati-
function 2
After re-allocation

FIG 12

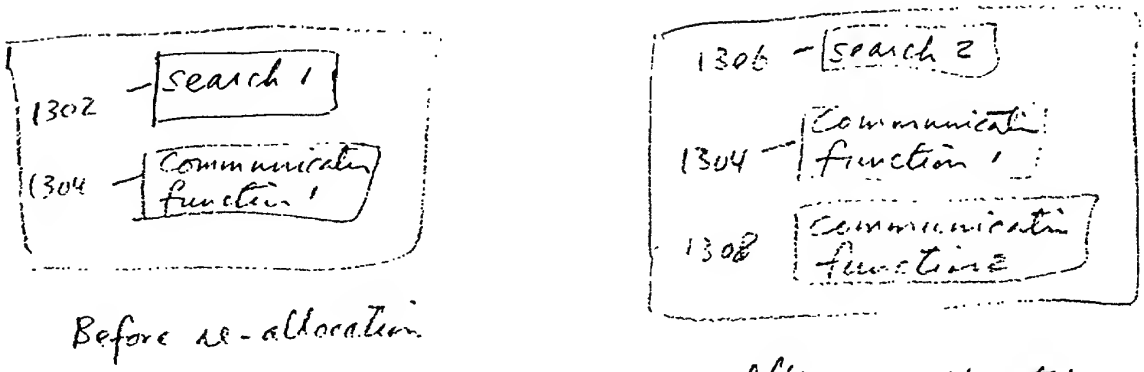

1302
search 1
1304
Communicati-
function 1
Before re-allocation
1306
search 2
1304
Communicati-
function 1
1308
Communicati-
function 2
After re-allocation

FIG. 13